We claim:

1. A method of operating a memory management system to resolve contention for access to a plurality of memories; said method comprising the steps of:

generating requests for the reading and writing of data by said memories;

generating signals indicating the busy / idle state of each of said memories;

extending said signals to an access flow regulator;

operating said access flow regulator in response to said receipt of said signals to determine the present busy / idle state of each of said memories;

applying said requests to said access flow regulator; and

operating said access flow regulator in response to a determination that one of said memories is currently idle for granting a request to for the reading or writing of a data by said one memory.

2. The method of claim 1 including the further steps of:

operating said access flow regulator in response to a determination that none of said memories is currently idle for buffering said request to define a buffered request until one of said memories becomes idle; and

serving said buffered request when said one of said memories becomes idle.

3. The method of claim 1 including the further steps of:

determining that a plurality of requests are concurrently seeking access to an idle one of said memories;

granting one of said requests access to said idle memory; and

buffering the other of said requests until one of said memories becomes idle and available to serve said other request.

4. The method of claim 1 wherein the step of generating includes the steps of:

monitoring the present busy / idle state of each of said memories;

generating a busy signal for a memory only for the time duration the memory is in a busy state;

generating an idle signal for a memory immediately upon a determination that the memory has assumed and idle state;

extending said idle signal to said access flow regulator; and

operating said access flow regulator to grant a waiting request access to said memory immediately upon the receipt of said idle signal by said access flow regulator.

5. The method of claim 1 wherein said system further comprises a plurality of state controllers each of which is individual to one of said memories, said system further comprises a request bus connecting said access flow regulator with said state controllers; said step of transmitting a read request includes the steps of:

operating said access flow regulator to select an idle one of said memories that is to receive a request;

transmitting said request from said access flow regulator over said request bus to the state controller individual to said idle one of said memories;

extending said request from said state controller to said idle memory individual to said state controller; and

operating said state controller to control the operation of the memory unique to said state controller.

6. The method of claim 5 wherein said step of operating said state controller includes the steps of:

determining the present occupancy level of said memory;

transmitting said request to said memory if said present occupancy level is not exceeded; and

buffering said request in said access flow regulator if said occupancy level of said selected memory is exceeded.

7. The method of claim 1 including the further steps of:

embodying said system into a network node having incoming and outgoing links;

applying requests received by said links to said access flow regulator; and

processing said requests for access to control the data throughput of said network node.

8. The method of claim 1 including the further steps of:

operating said system to concurrently process a plurality of requests for access to idle ones of said memories; and

buffering said requests that are received when an idle one of said memories is not available.

9. The method of claim 5 wherein said step of extending said signals to said access flow regulator includes the steps of:

extending said signals over separate conductors to said access flow regulator with each of said conductors being individual to a different one of said memories; and

operating said access flow regulator to detect the signal on each conductor to determine the busy / idle state of the memory unique to each conductor.

10. The method of claim 9 including the further steps of:

extending said signal over said separate conductors from said state controllers to said access flow regulator, each conductor extends between said access flow regulator and a different one of said state controllers.

11. A memory management system for resolving contention for access to a plurality of memories; said system comprising:

apparatus for generating requests for the reading and writing of data by said memories;

apparatus for generating signals indicating the busy / idle state of each of said memories;

apparatus for extending said signals to said access flow regulator;

apparatus for operating said access flow regulator in response to said receipt of said signals to determine the present busy / idle state of each of said memories;

apparatus for applying said requests to an access flow regulator; and

apparatus for operating said access flow regulator in response to a determination that one of said memories is currently idle for granting a request to for the reading or writing of a data by said one memory.

12. The system of claim 11 further including:

apparatus for operating said access flow regulator in response to a determination that none of said memories is currently idle for buffering said request to define a buffered request until one of said memories becomes idle; and

apparatus for granting said buffered request when said one of said memories becomes idle.

13. The system of claim 11 further including:

apparatus for determining that a plurality of requests are concurrently seeking access to an idle one of said memories;

apparatus for granting one of said requests access to said idle memory; and

buffering the other of said requests until one of said memories becomes available to serve said other request.

14. The system of claim 11 further including:

apparatus for monitoring the present busy / idle state of each of said memories;

apparatus for generating a busy signal only for the time duration a memory is in a busy state;

apparatus for generating an idle signal immediately upon a determination that a memory has assumed and idle state;

apparatus for extending said idle signal to said access flow regulator; and

apparatus for operating said access flow regulator to grant a waiting request access to said memory immediately upon the receipt of said idle signal by said access flow regulator.

15. The system of claim 11 further comprising:

a plurality of state controllers each of which is individual to one of said memories;

a request bus connecting said access flow regulator with said state controllers;

apparatus for operating said access flow regulator to select an idle one of said memories that is to receive a request;

apparatus for transmitting said request from said access flow regulator over said request bus to the state controller individual to said idle one of said memories; and

apparatus for extending said request from said state controller to said idle ones of said memories.

16. The system of claim 15 wherein said apparatus for operating said state controller includes:

apparatus for determining the present occupancy level of said memory;

apparatus for transmitting said request to said memory if said present occupancy level is not exceeded; and

apparatus for buffering said request in said access flow regulator if said occupancy level of said selected memory is exceeded.

17. The system of claim 15 further including:

apparatus for embodying said system into a network node having incoming and outgoing links;

apparatus for applying requests received by said links to said access flow regulator; and

apparatus for processing said information to control the data throughput of said network node.

18. The system of claim 11 further including:

apparatus for operating said system to concurrently process a plurality of requests for access to idle ones of said memories; and

apparatus for buffering said requests that are received when an idle one of said memories is not available.

19. The method of claim 13 wherein said apparatus for extending said signals comprises:

apparatus for extending said signals over separate conductors to said access flow regulator, each of said conductors is individual to a different one of said memories; and

apparatus for operating said access flow regulator to detect the signal on each conductor to determine the busy / idle state of the memory unique to each conductor.

20 The method of claim 19 further includes:

apparatus for extending said signal over said separate conductors from said state controller to said access flow regulator from said state controllers, each said conductor extends between said access flow regulator and a unique on of said state controllers.

5